ECE/ME 541 Spring 07, Feinerman, Final solutions, 5/9/08, ***Closed* Book** & **Notes** $\bar{x}$ = 63.0, σ = 19.2

II	III	IV	V	VI
	B	C	N	O
	Al	Si	P	S
Zn	Ga	Ge	As	Se
Cd	In	Sn	Sb	Te

*Avogadro's Number, N_{Av} = 6.022*10^{23} atoms/mole, Boltzmann's constant, k_B = 1.3807*10^{-23} J/°K*
*eV = 1.602*10^{-19} J, e = 1.602*10^{-19} coulombs, c = 2.998*10^{8} m/s, h = 6.626*10^{-34} J*s,*
*ε_o=8.854*10^{-14} Fd/cm, 1nm = 10^{-3} μm = 10^{-6} mm = 10^{-7} cm, **Silicon** n_i=1.41*10^{10}/cm^3, K_S=11.8,*
E_g=1.12eV. $n*p=n_i^2$ (non-degenerate semiconductors), $R=\rho*\frac{L}{w*t}$

$$C(x,t)=\frac{Q}{\sqrt{\pi Dt}}\exp\left(-\frac{x^2}{4Dt}\right),\quad Q=\int_0^\infty C(x,t)*dx \quad \textbf{Constant dopant}$$

$$C(x,t)=C_S\left[erfc\left(\frac{x}{4\sqrt{Dt}}\right)\right],\quad Q=\int_0^\infty C(x,t)*dx=\frac{2C_S}{\sqrt{\pi}}\sqrt{Dt} \quad \textbf{Constant source}$$

$$(D*t)_{total}=(D*t)_1+(D*t)_2+\ldots \quad n_i=3.9\times10^{16}T^{3/2}\exp\left(-\frac{0.605}{k_B*T}\right),\ \text{Ideal gas law, } P*V=N*k_B*T,$$

$$C(x)=\frac{Q}{\sqrt{2*\pi}*\Delta R_p}\exp\left(-\frac{(x-R_p)^2}{2*\Delta R_p^2}\right) \quad \textbf{ion implantation},\quad Q=\int_{-\infty}^{\infty}C(x)*dx,\quad \nabla\bullet\vec{E}=\frac{\rho}{\varepsilon_r*\varepsilon_o}$$

1) *Does the industry.'s efforts to follow "Moore's law" favor ion implantation, diffusion, or neither and why or why not ?* $\bar{x}$ =8.5, σ =3.4

"Moore's law," favors ion implantation because they need to make smaller devices with shallower junction depths.

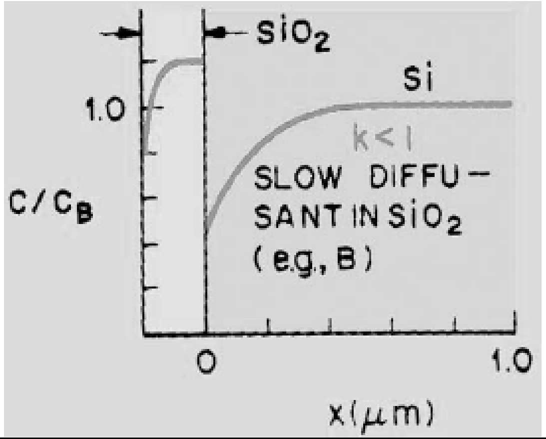
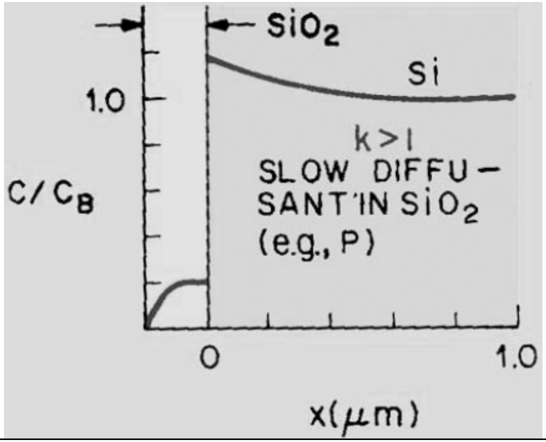
2) *Why does the oxidation ~~rate~~ thickness change from being proportional to the oxidation time to being proportional to the square root of the time ?* $\bar{x}$ =2.5, σ =4.2

Initially the oxidation rate is limited by the reaction at the surface, so the thickness depends on the total number of oxygen atoms arriving at the surface which is proportional to oxidation time. After the oxide thickness has increased the rate limiting step is diffusion of the oxidant through the oxide. The time to diffuse through oxide is proportional to the oxidation thickness squared. $x_{ox}\propto\sqrt{D*t_{ox}}$. If you look at the oxidation equation $B=\frac{2*D*C^*}{N_1}$, and $\frac{B}{A}=\frac{C^* * k_S}{N_1}$

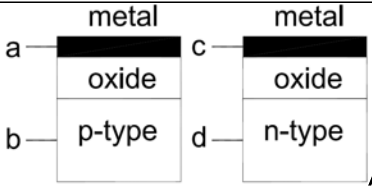
where N_1 = # oxidant molecules incorporated per cc of oxide, C^* is oxidant concentration in a piece of oxide in the furnace, D is the diffusion coefficient, and k_S is the surface reaction rate.

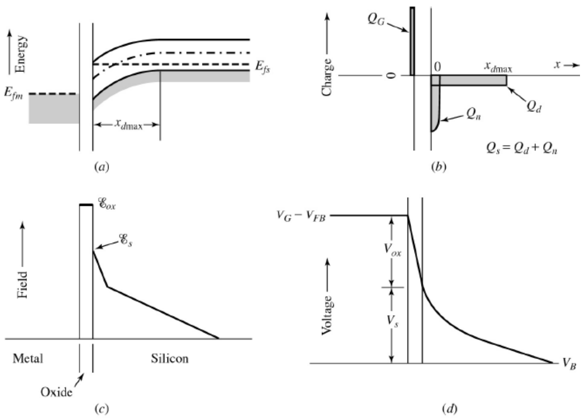
3) *List **two** effects that can happen when oxidizing doped silicon and indicate how this can change device performance.* $\bar{x}$ =3.0, σ =1.8

Question looked for four items. a) variations in dopant incorporation in oxide leading to pile-up or depletion at the Si/SiO$_2$ interface. b) variations in oxidation rate leading to non-uniform thickness of gate oxide, c) changing doping at Si/SiO$_2$ interface under gate changes channel resistance and device speed, d) changing doping at Si/SiO$_2$ interface and thickness of gate oxide leads to variations in threshold voltage.

	
P-type dopants tend to segregate into the SiO$_2$ which lowers the doping in the silicon immediately below the Si/SiO$_2$ interface.	N-type dopants tend to segregate into the silicon which increases the doping in the silicon immediately below the Si/SiO$_2$ interface.

4) *How can we electrically invert the surface of the silicon (silicon/oxide interface)* ***?*** *(hint: what has to happen with contacts at a, b, c, and d).* $\bar{x}=7.5, \sigma=3.5$

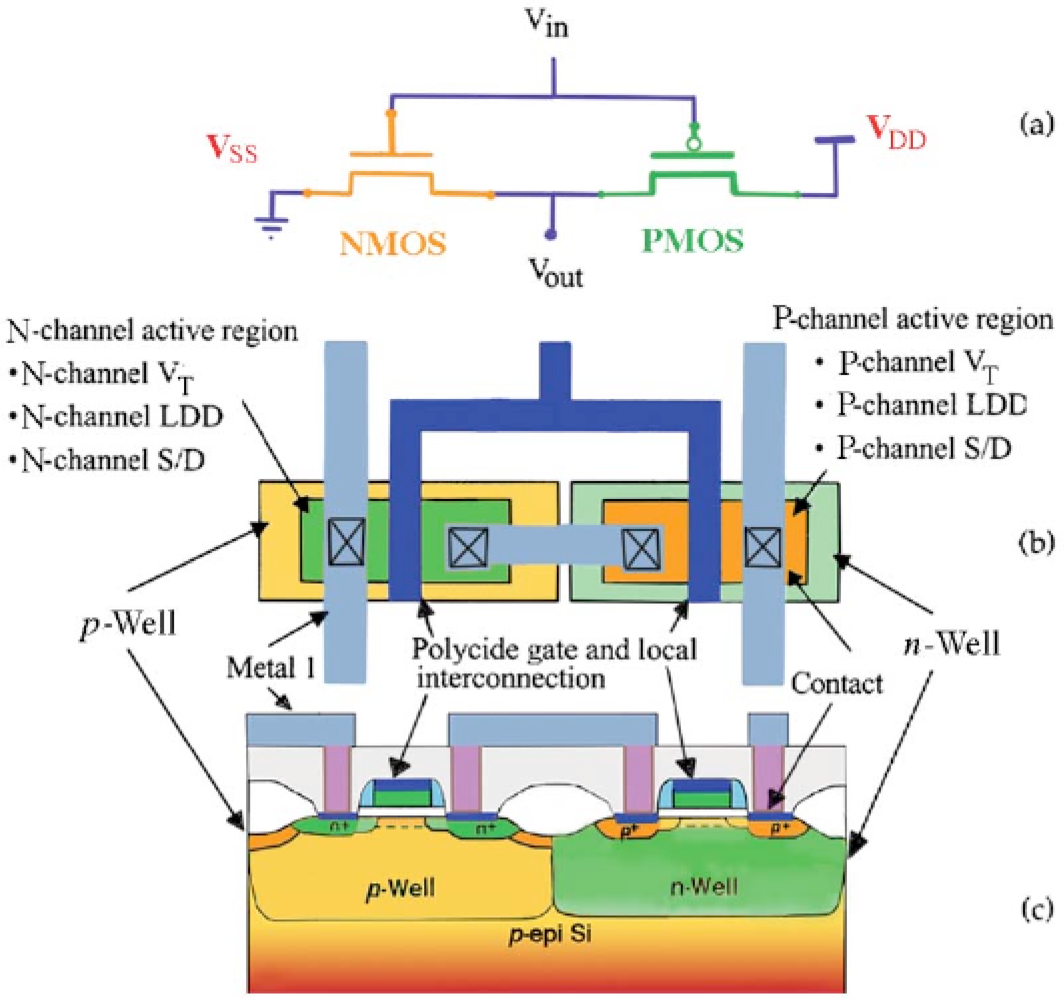




Applying a sufficient positive voltage (V_a-V_b = V_g>V_{tn}) to the gate above a p-type channel creates an electric field that pulls electrons to the surface. The electric field causes the bands to bend down until the Fermi level crosses the intrinsic level. Applying a sufficient negative voltage (V_c-V_d = V_g<V_{tp}) to the gate above an n-type channel creates an electric field that pulls holes to the surface.

5) *How is it possible without consuming a great deal of power to simultaneously electrically invert both n-type and p-type silicon surfaces on the same wafer* ***?*** *(a picture might clarify your answer).* $\bar{x}=3.5, \sigma=2.8$

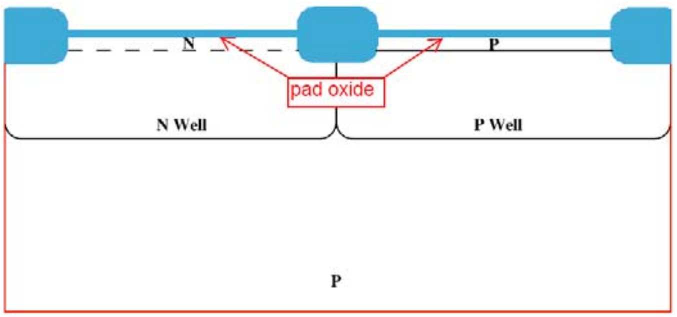
Question looked for understanding that reverse biased PN junctions don't draw significant current. Usually the p-well is at 0 volts and the n-well is at V_{DD} (~+5 volts), so no current flows **since the two adjacent wells form a diode that is kept reverse biased with V_d > V_b**. As shown below the gates in a CMOS inverter are shorted, and when both gates are at 0 volts, then the p channel over the n-well is inverted, and there is no n-channel over the p-well. If both gates are at +V_{DD}, then the n channel over the p-well is inverted, and there is no p-channel over the n-well. If both gates are at ~$V_{DD}/2$ (which happens when inverter input switched from low to high or high to low) then both channels invert and there is a brief spike of current drawn from the V_{DD} supply through the channels. There is always minimal current through the wells because they are reverse biased.



CMOS inverter: (a) *Circuit-diagram* form;
(b) *Layout* form; (c) *Physical* form (in cross-section)

6) *Give two reasons why the pad oxide is stripped and replaced with a gate oxide of approximately the same thickness? Identify the pad oxide in the following figure.* $\overline{x} = 6.3$, $\sigma = 3.1$

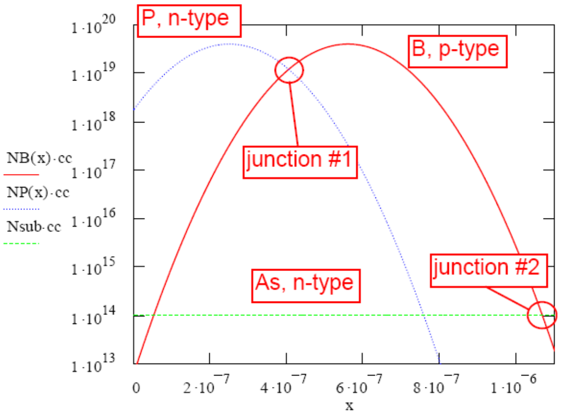
Pad oxide was damaged by well and threshold adjust implants so stripping pad oxide and growing new oxide produces higher quality gate oxide. Original pad oxide was too thick (~40nm) to be gate oxide (3-5nm).



7) *The ion implanter operator was surfing the web instead of paying attention to his run sheet and implanted Boron, Silicon, and then Phosphorous. The wafer he implanted into was uniformly doped with Arsenic at 10^{14}/cm^3. Each species was implanted to a concentration of 10^{15}/cm^2 and with the parameters in the following table. Where did the operator place the junction(s) if any? Please answer the following questions:* $\bar{x} = 13.9$, $\sigma = 7.7$

   a) *qualitative sketch of the impurity distributions*
   b) *the surface doping level ($N_s = \Sigma N_a - \Sigma N_d$)*
   c) *the exact location of each (or any) junction.*

Species	*Range, R_p*	*Straggle, ΔR_p*
B	*0.56μm*	*0.10μm*
Si	*0.10μm*	*0.05μm*
P	*0.25μm*	*0.10μm*



Implanted silicon is not considered a dopant so it can be ignored. There are three impurity distributions and two junctions. Arsenic - n-type - NAs(x) = 10^{14}/cc,

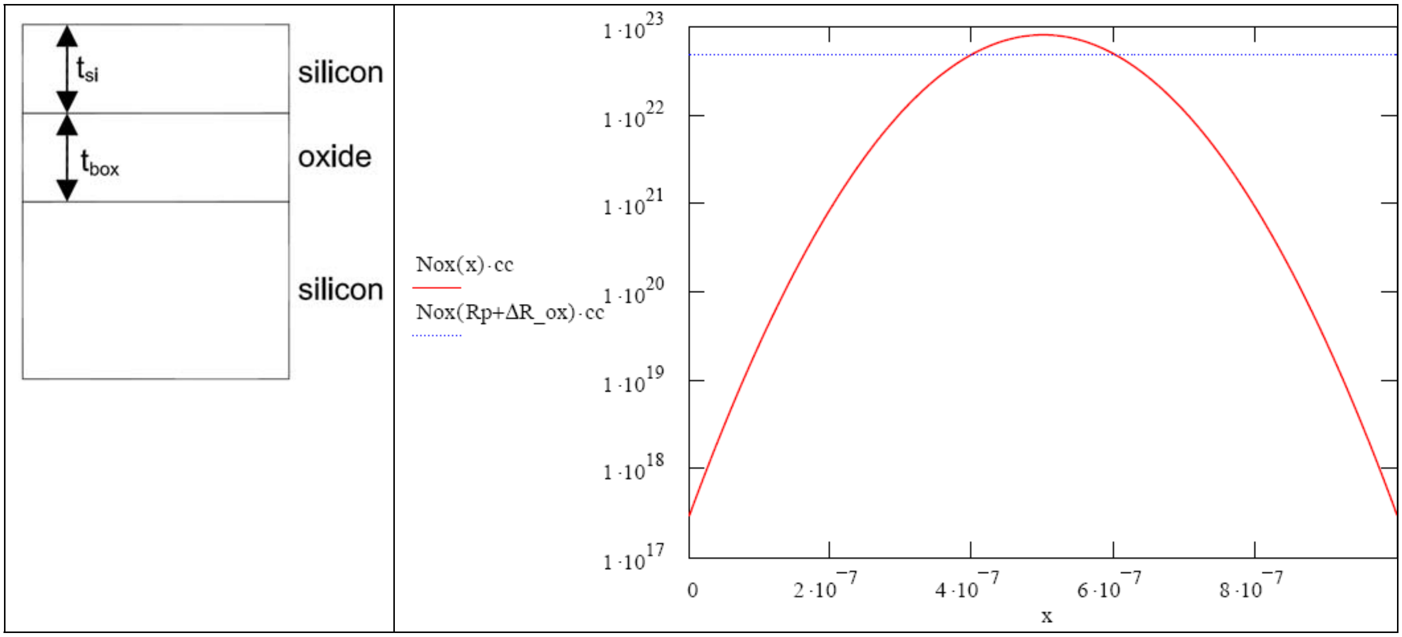
Phosphorous – n-type - $NP(x) = N_{peak}\exp\left(-\frac{(x-R_{p1})^2}{2*\Delta R_p^2}\right)$,

and Boron – p-type - $NB(x) = N_{peak}\exp\left(-\frac{(x-R_{p2})^2}{2*\Delta R_p^2}\right)$

$N_{peak} = \frac{Q}{\sqrt{2*\pi*\Delta R_p}} = \frac{3.989*10^{19}}{cc}$, and ΔR_p=0.1μm, R_{p1}=0.25μm, and R_{p2}=0.56μm. Surface concentration is n-type and $NAs + NP(0) - NB(0) \cong NP(0) = \frac{1.75*10^{18}}{cc}$. Junction 1 is where $NB(x_{j1}) = NAs + NP(x_{j1}) \cong NP(x_{j1})$, which is easily solved to be $x_{j1} = \frac{R_{p1}+R_{p2}}{2} = 0.405\mu m$. As a check NP($x_{j1}$) = NB($x_{j1}$) = $1.20*10^{19}$/cc >> NAs. Junction 2 is where $NB(x_{j2}) = NAs + NP(x_{j2}) \cong NAs$, which is easily solved to be x_{j2} = 1.07μm. As a check NB(x_{j2}) = 10^{14}/cc = NAs. Grading, 7 points for sketch and 6 points each for surface doping, x_{j1}, and x_{j2}.

8) *You need to make an SOI wafer (silicon on insulator). Your implanter can deposit 20 mA of O^+ ions at 200 keV. The range (R_p) and projected straggle (ΔR_p) of these ions is 500nm and 100nm respectively. You can assume the formation of SiO_2 doesn't happen during the implant, that the oxidation will occur symmetrically about the peak of the distribution, $n_{Si} = 5.0*10^{22}$/cc, $n_{SiO2} = 2.2*10^{22}$/cc, and $t_{si}/t_{ox} = 0.44$* $\bar{x} = 2.4$, $\sigma = 5.1$

   a) *What flux of oxygen ions (Q) is needed to form a buried oxide layer* ***?*** *(Hint: assume oxidation will only occur between $R_p - \Delta R_p$ and $R_p + \Delta R_p$ and that this includes 68% of ion distribution)*
   b) *How long does it take to implant a single 12 inch diameter wafer* ***?*** *(area = 730cm^2)*
   c) *How much power heats this wafer during the implantation* ***?*** *Will wafer cooling be necessary* ***?***
   d) *How large are t_{si} and t_{box} after the oxidation* ***?*** *(t_{box} refers to buried oxide layer)*
   e) *What flux of low energy oxygen ions (Q) is needed if a 10nm gate oxide has to be formed* ***?***



a) Since $68\% * Q = \frac{2oxygen}{SiO_2} * nSi * (2 * \Delta R_p)$, Q=2.94*10^{18}/cm^2.

b) Since $I_{beam} * \tau = e * Q * Wafer\_area$, τ=4.77 hours

c) Power = current * voltage = I_{beam}*200kV = 4000 watts. This is in vacuum, so cooling is critical !

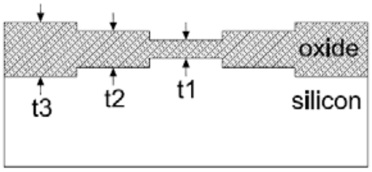
d) $t_{si} = R_p - \Delta R_p$ = 400nm, $t_{box} = \frac{2 * \Delta R_p}{0.44} = 455nm$

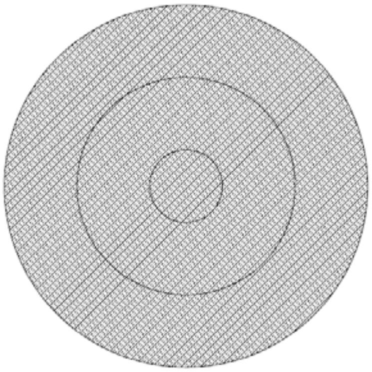
e) 4.4nm of silicon forms 10nm oxide, $100\% * Q = \frac{2oxygen}{SiO_2} * nSi * 4.4nm = \frac{4.4 * 10^{16}}{cm^2}$

This process is called SIMOX **S**eparation by **IM**plantation of **OX**ygen. Oxide grows mainly on near side of peak not symmetrically as stated to make problem easier to solve. Devices can be electrically separated by oxide instead of by thick depletion regions between reverse biased junctions. Grading, 5 points each for a - e.

9) *Outline a process to create the structure in the following figure with t1 = 0.5μm, t2 = 1.0μm, and t3 = 1.5μm. You can assume B = 0.500μm^2/hour, and B/A = 4.20μm/hour, and that the circles*

have diameters of 100, 300, and 500μm. Is the top surface of the silicon sketched correctly (is the surface of the middle circle higher than the surface of the outer circle, etc.) **?** $\bar{x}=16.0,\ \sigma=4.6$





$$\frac{t_{ox}^2}{B}+\frac{t_{ox}}{B/A}=t+\tau$$ *Deal-Grove model*

$ax^2 + bx + c = 0$, -> $x=\dfrac{-b\pm\sqrt{b^2-4ac}}{2a}$

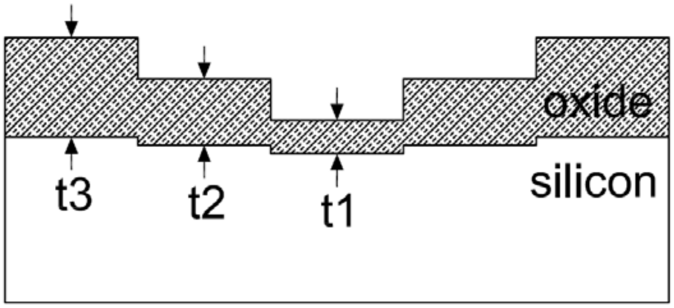
Side view *top view*

Since $\frac{t_{ox}^2}{B}+\frac{t_{ox}}{B/A}=t+\tau$, then τ_3 = 4.86 hours to grow t3, τ_2 = 2.24 hours to grow t2, and τ_1 = 0.619 hours to grow t1. A procedure to make structure would be to

1) Oxidize for **(τ_3 – τ_2) = 2.62 hours**, then etch oxide from inner and middle circles.
2) Oxidize for **(τ_2 - τ_1) = 1.62 hours**, and then etch oxide from inner circle,
3) Oxidize for **τ_1 = 0.619 hours**.

Each region gets the correct oxidation time. In the regions where the oxide is etched and then a new oxide is grown, the new oxide will grows faster than areas where the oxide wasn't etched. The correct profile would be as follows. Several students proposed instead a more cumbersome process:

1) oxidizing wafer for **τ_1 = 0.619 hours**.
2) masking inner circle, and oxidizing rest of wafer for middle circle for **(τ_2 - τ_1) = 1.62 hours**, The only mask that can withstand oxidation is LPCVD nitride.
3) Masking inner and middle circles and oxidizing rest of wafer for **(τ_3 – τ_2) = 2.62 hours**. If you follow this process this then the cross-section previously given is correct.



Grading, 5 points each for correct process, three oxidation times, and correct cross-section.